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(use as may sheets as necessary)

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Complete if Known	
Application Number	
Filing Date	August 20, 2003
First Named Inventor	Viktor Koldiaev
Group Art Unit	
Examiner Name	
Attorney Docket Number	88103.0001

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		Chin-hsing Yu, et al., Ultrathin (2.7nm) Oxy-nitride for Suppressing Boron Penetration Characterized by Direct Hole Tunneling Current in p+/pMOS, Technology Development Center, Worldwide Semiconductor Manufacturing Corp., Hsinchu, Taiwan 30077, Republic of China	
		S.C. Song, et al., Ultra Thin high quality stack nitride/oxide gate dielectrics prepaed by *in-situ* rapid thermal N_20 oxidation of NH_3-nitrided Si, Mecroelectronics Research Center, Department of Electrical and Computer Engineering The University of Texas, Austin, TX	
		Quazi D. M., Khosru, et al., Low Thermal-Budget Ultrathin NH_3-Annealed Atomic-Layer-Deposited Si-Nitride/$Si0_2$ Stack Gate Dielectrics With Excellent Reliability, IEEE Electron Device Letters, Vol. 23, No. 4, April 2002	
		Quazi D.M., Khosru, et al., Ultrathin NH_3 Annealed Atomic Layer Deposited Si-nitride/Si02 Stack Gate Dielectrics with High Reliability, Research Centr for Nanodevices and Systems, Hiroshima University, 1-4-2 Kagamiyama, Higashi-Hiroshima, Japan	

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